Yield improvement in Semiconductors

Purpose of the paper is to show that yield improvement is multifaceted and all major components for yield improvement are essential for rapid yield ramp.

The yield improvement process involves several steps and typically evolves as follows:

1. Silicon debug and design marginality.
2. Data analysis to understand most failing structures.
3. Fail site isolation (EFA) using memory physical to logical, liquid crystal, photoemission microscopy and logic mapping.
4. Physical failure analysis of the failing structures to understand cause of failure.
5. Building up failure statistic.
6. Report main causes of failure (pareto) for process improvement.

The process of yield improvement is continuous and the role of data and failure analysis is essential. With good data analysis, failure analysis, and failure pareto, many a times yield improvement is only marginal. It is becoming essential with newer technologies that other methods such as logic fails, constructional analysis and comparisons of data between foundries may facilitate highlighting problem areas. Examples of such marginal improvement even with good data analysis, EFA and PFA will be discussed.

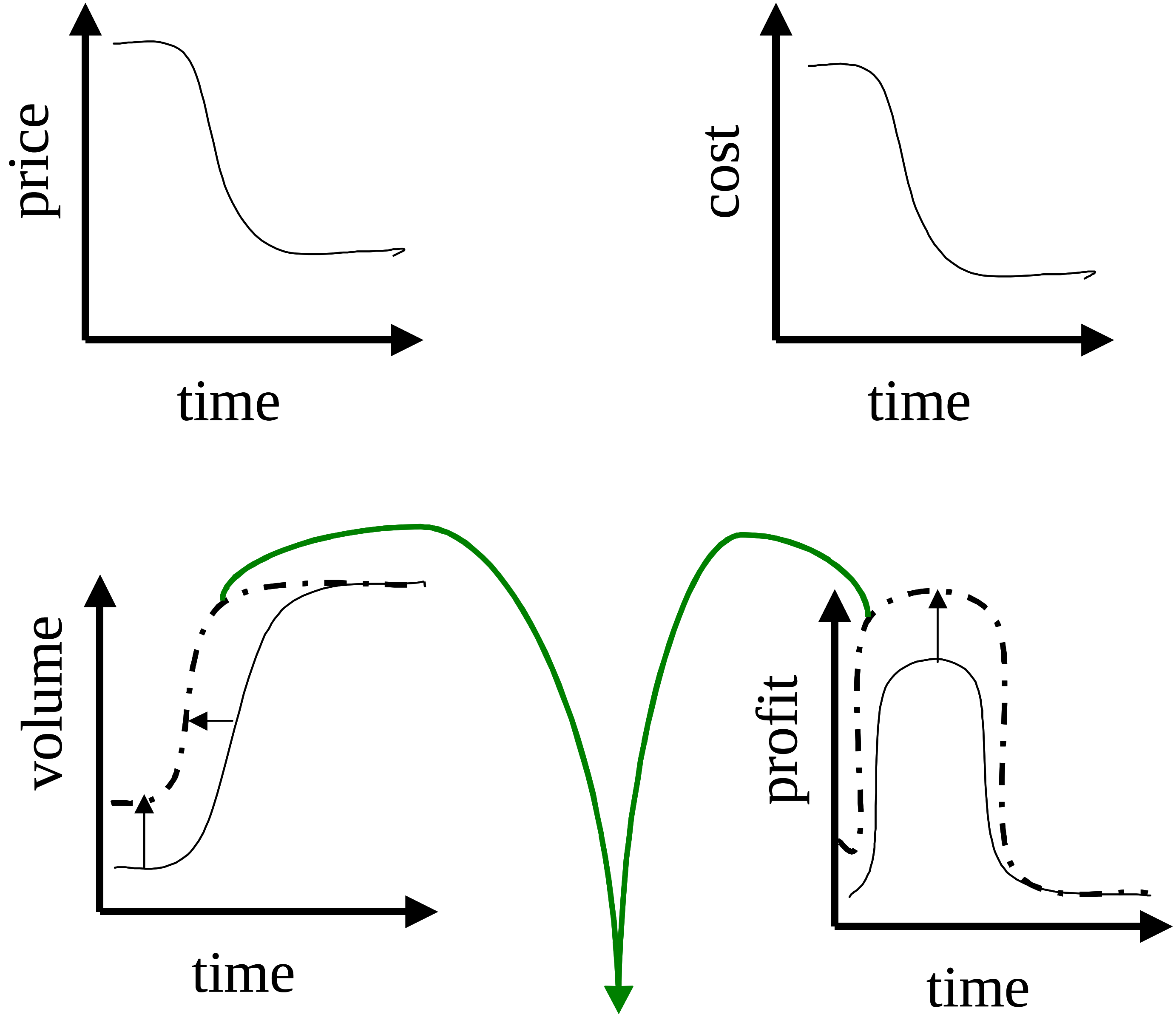
Components that will be discussed include:

1. Data analysis
2. Fail pareto analysis
3. Constructional analysis (comparisons of some critical layers between foundries)

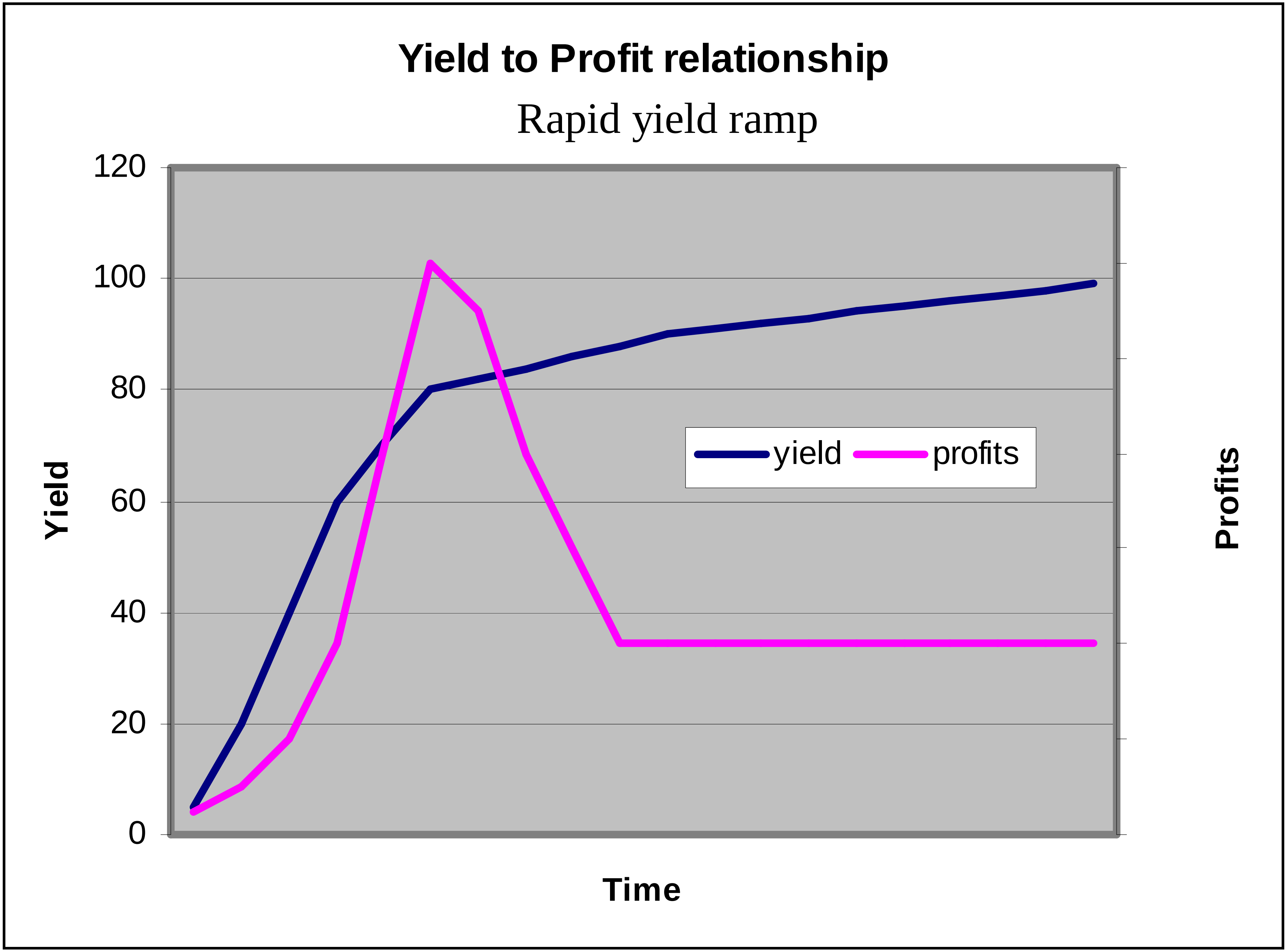
Introduction

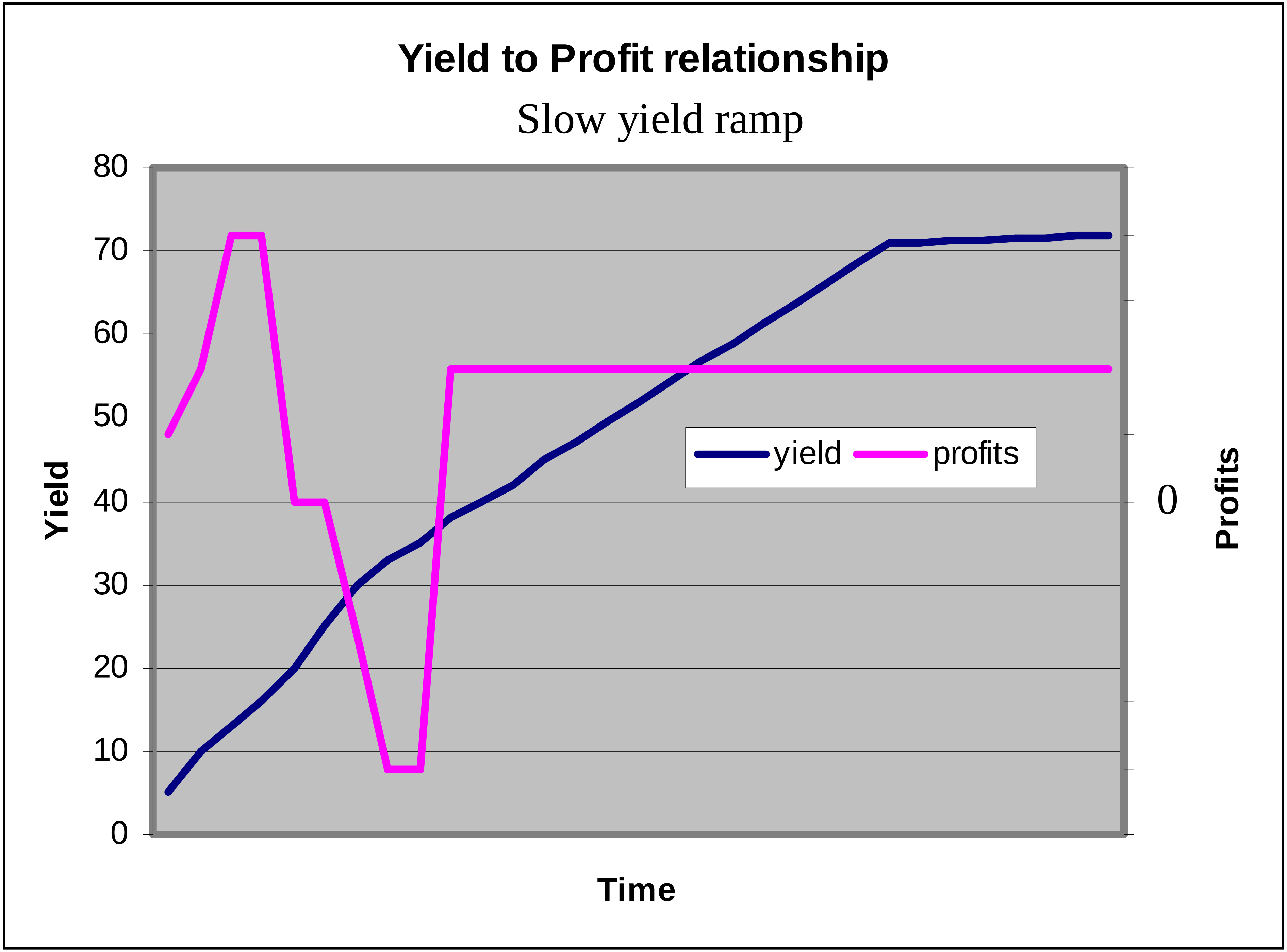
- Yield: Yield is the percentage functional dies produced per wafer.
- Yield problems can be:
  - Random defects
  - Systematic defects
  - Misprocessing
  - Design

Time, Yield, cost and Profit



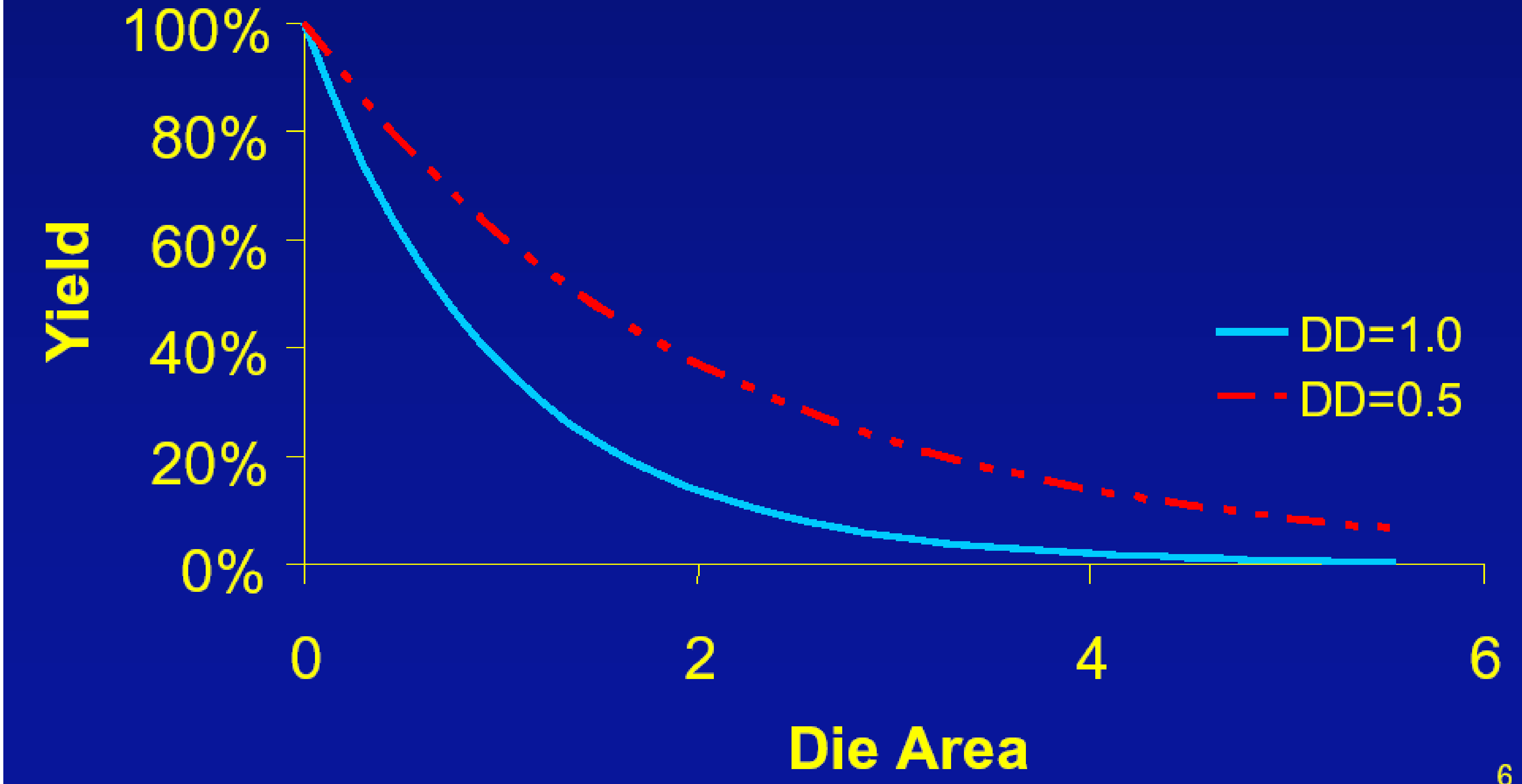
Improve Yield -> Increase Profits


Yield to Profit relationship
Rapid yield ramp
120
100
80
60
40
20
0
Yield
Profits
Time
yield
profits


Yield to Profit relationship
Slow yield ramp
80
70
60
50
40
30
20
10
0
Yield
yield
profits
0
Profits
Time

Yield Modeling

Comparison of yield response curves for different defect densities using the Poisson Model.



Yield Modeling

- For a typical range of die sizes

	Area = 0.5	Area = 1.0	Difference
DD=0.5	77.9%	60.7%	17.2%
DD=1.0	60.7%	36.8%	23.9%
Difference	17.2%	23.9%	

- Values will vary depending on the area of the chip.

Yield Analysis

- First step in yield improvement is to understand the yield status.
- Two types of yield improvements:
  - Baseline yield improvement
    - Need baseline yield improvement in
      - new products
      - New process development
  - Excursion control
    - Can be due to
      - Equipment break down
      - Human error (misprocessing)

Yield improvement at 0 to 50%

- Yield loss mainly due to improper centering of process parameters such as gate CD, contact CD, ILD thicknesses, etc. Centering of transistor parameters such as I drives, Ioffs and CGD is also critical.
- Significant yield loss due to product issues such as incorrect silicon PG, photo marginality and dense to isolated bias.
- PFA in this region should support process integration in checking issues related to parametric centering such as CDs, thicknesses, step heights, etc.

Yield improvement in the 50 to 80%

- This yield improvement is the hardest.
- It requires a robust beginning (sound technology, integration and process/product marginality).
- PFA should support activities defining
  - regions of the wafer that are bad (edge vs center, top vs bottom)
  - Perform PFA from the most failing bin (logic to SRAM). But when yield approaches 50%, significant yield loss is from logic. Logic is mostly isolated.
  - Perform critical assessment of the two regions with different yields.
  - Compare to external foundries (if available) process issues.
  - Use DD vehicles for more statistics from fail region.
  - Maintaining a consistent process.

Yield improvement in >80%

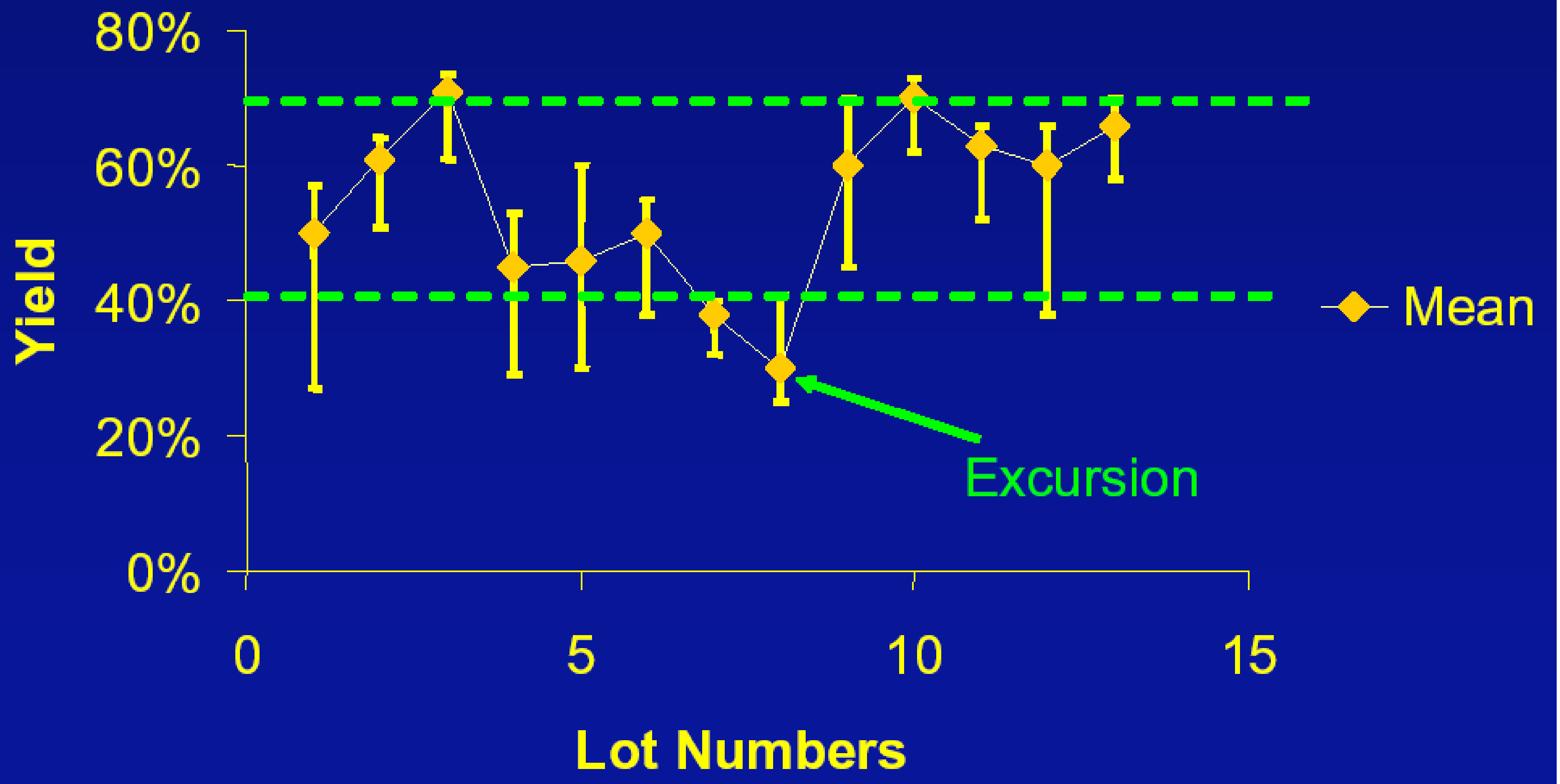
- Extremely tight SPC controls on each process step.
- Mostly defect driven fails. So put more emphasis on equipment DD reduction.

Data Mining

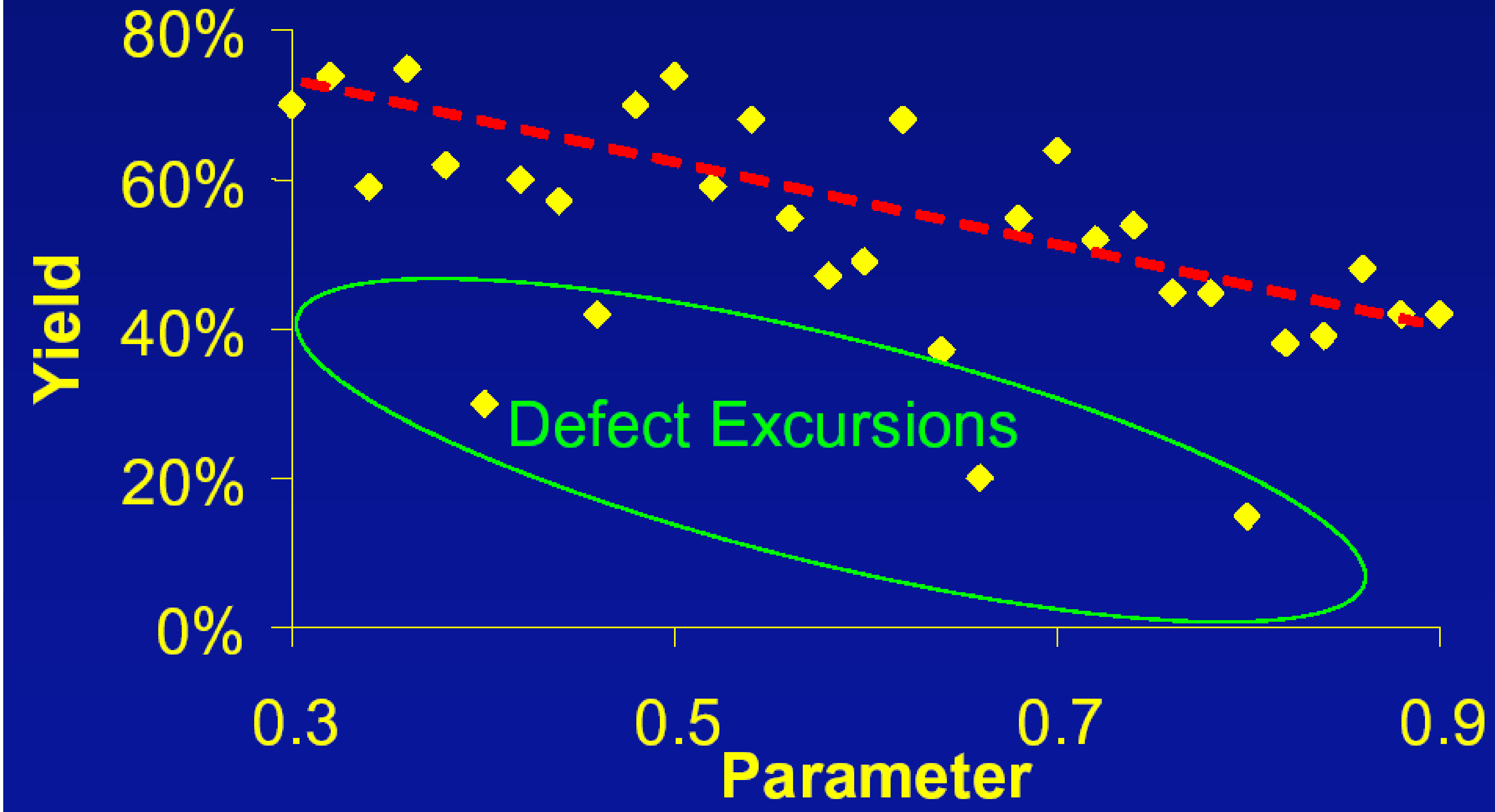
- Data mining is one of the tools for yield improvement.
- Typically used as a first step in the yield improvement process to isolate failure site (location).
- Data mining to understand:
  - Test related issue. Test flow and binning.
  - Specific location of wafer is a hot spot (center or edge)
  - SRAM analysis to understand specific level (loop) is failing. (Gate, contact, M1, etc.)
  - Parametric to functional correlation. (OCP to functional, scribe parametrics to functional)
  - Inline defect map to end of line correlation.
- After data mining, PFA is performed to drill down to the exact root cause.

Yield Analysis

- Yield trend charts help to identify baseline trends and major yield excursions.

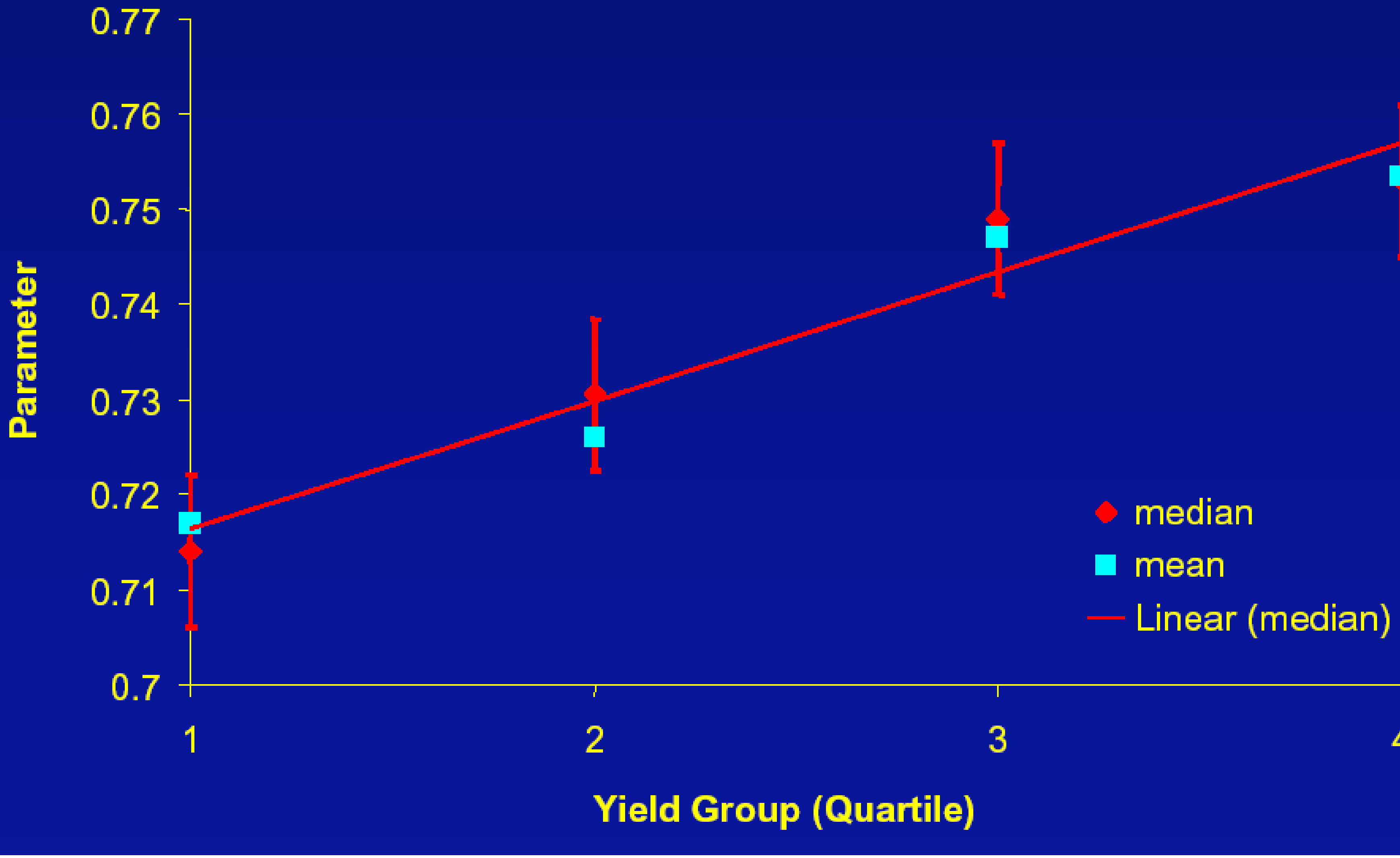


Parametric Analysis for Yield



Parametric Analysis for Yield

- Statistical results from search for electrical parameters which correlate with yield.



Testing

- Understanding of test flow.
- Is most failing structure being tested.
- Schmoo of most failing structure (SRAM vs logic).
- Is it voltage sensitive.
- Is it frequency sensitive.
- Is Iddq marginal or high. Is this due to a particular structure (example Nmos is leakier than Pmos)
- Can structure be a reliability issue.
  - Time zero fail vs field failure.
- Is logic mapping available (ATPG)

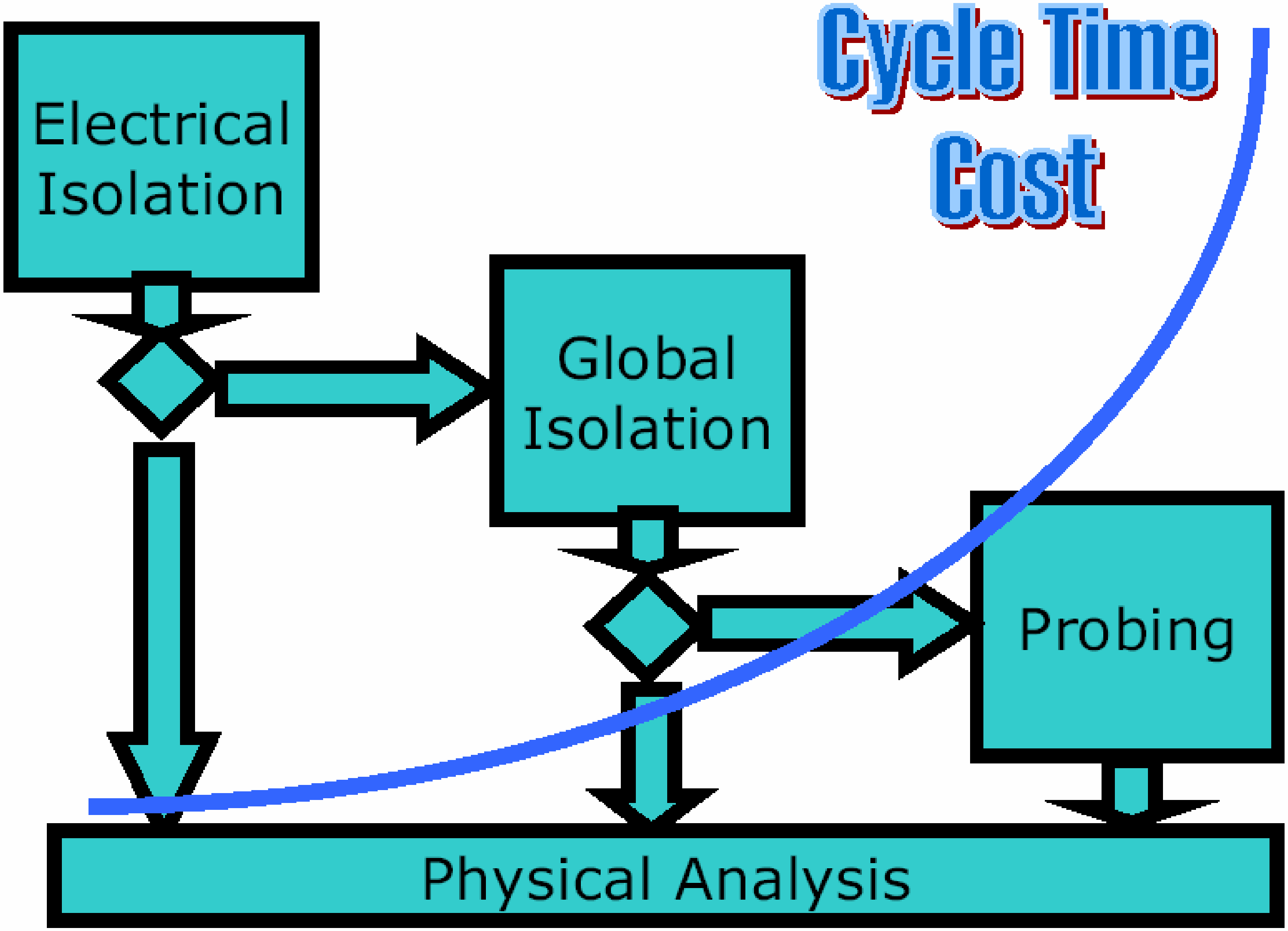
EFA & PFA

You must know where to look and what you are looking for especially when there are over 1million gates.

Failure Analysis

- Failure analysis can play a very critical role in yield improvement.
- Failure analysis needs comprehensive knowledge of:
  - Testing
  - Layout
  - Data analysis to understand most failing structures.
  - Fail site isolation techniques
  - Physical Failure analysis techniques.

Failure Site Isolation



Cycle Time

Cost

Electrical Isolation

Global Isolation

Probing

Physical Analysis

Different fail site isolation methods

- Memory (logical to physical mapping)
  - The method while good, it does not take into account dense to isolated area differences which can be further enhanced by topology.
- Logic mapping.
  - This method has been proven to be good when the failing net is short (~$50\mu m^2$).
  - Not good for large failing nets. Typically a shorted fail will have large nets failing as it could involve two or more nets to fail.
  - Not good if there is no ATPG pattern to test.
- Liquid Crystal:
  - Can isolated large defects such as PO scratches, and ESD / EOS type fails but is not good to detect small fails such as via opens.
- Photoemission:
  - Excellent to detect shorts and opens (floating gates)
  - Needs good detector that can detect in the visible to Infrared range.

EFA using photoemission

- Two types of emissions are present in IC failures:
  - Hot electrons
  - Black body
- Hot electrons
  - Saturated electrons are slowed down suddenly due to a high resistive path. This causes electron emission. This kind of emission is observed in the following mechanisms:
    - Over Biased junction
    - Latch up
    - Floating gates
    - Hot transistors among other normal transistors. Emission contrast.
- Black Body
  - High resistance fails causes localized heating.
  - Shorts causing localized heating.

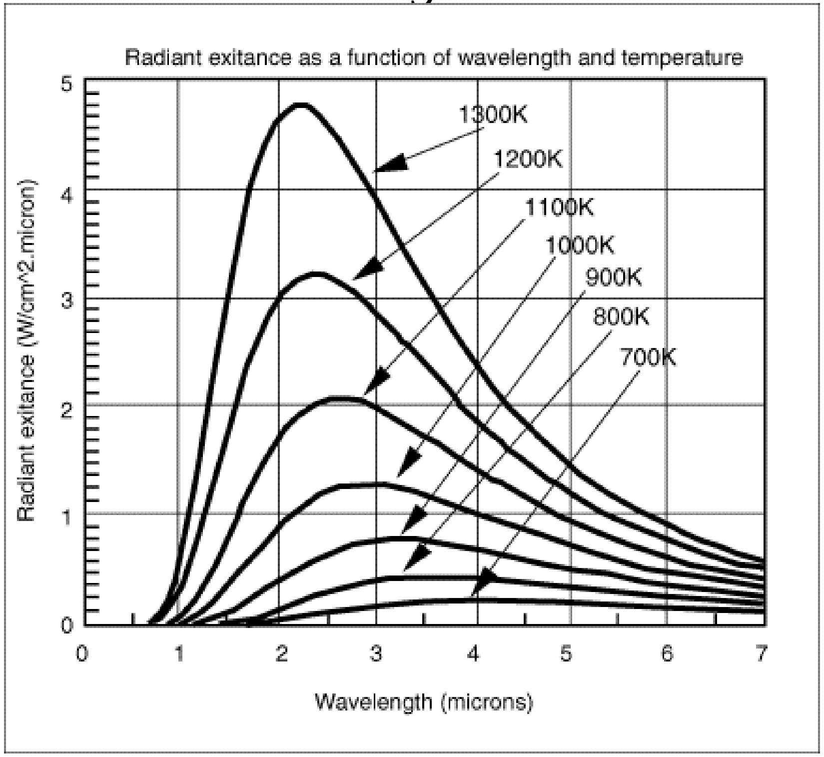
Hot Electron and Black Body Emit in entirely different regimes

- Hot electrons emit in the 620nm to 1300nm

$$\lambda = \frac{h\nu}{\phi} = \frac{1239.8}{E_g + E_a} = \frac{1239.8}{1.1 to 2.0} = 620 to 1130 nm$$

This is in the red light to near infrared region

Black body Radiation



- The wavelength of emission for black body is >1500nm (>1.5µm)
- Hence black body emission is in an entirely different region than hot electrons.
- Alpha innotech uses a silicon CCD to perform Near infrared imaging. CCDs loose their detective power past 1000nm.

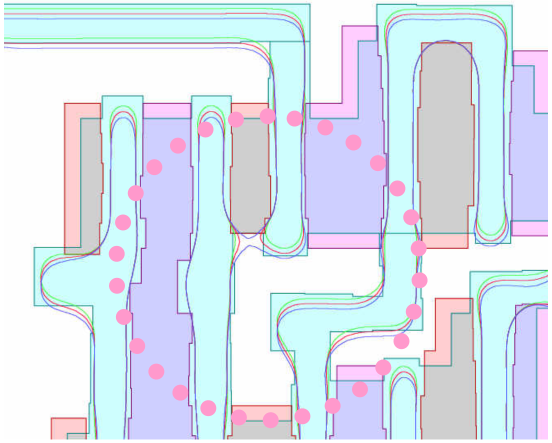
EFA

- Isolating the fail using one or few of the fail site isolation techniques is crucial in driving down to the failure.
- Using just one type of fail site isolation technique is insufficient.

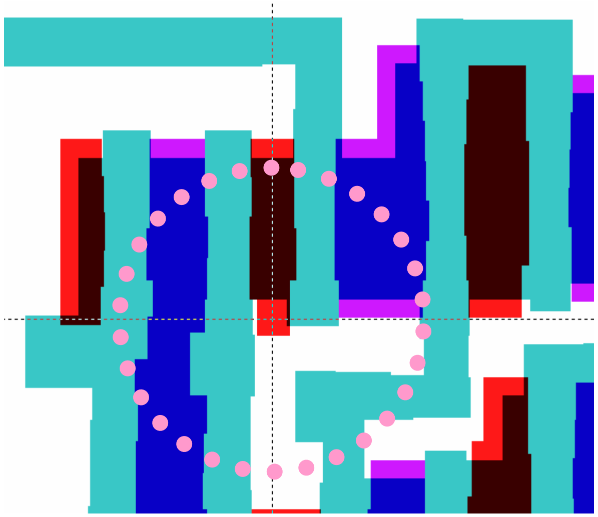
Silicon Debug

Gate Short Possible Root Cause for Bin 14 Failures

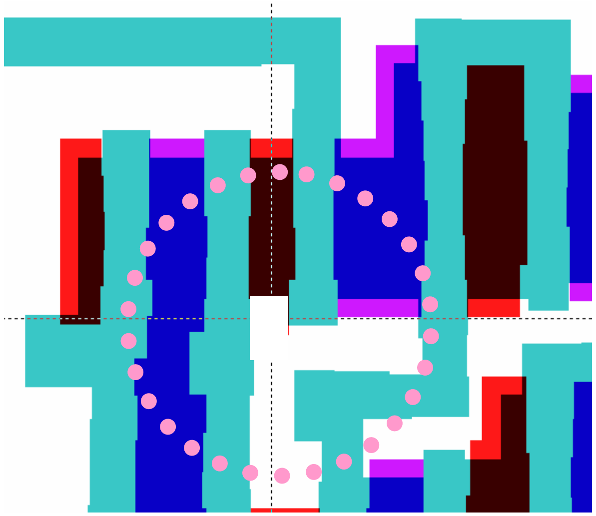
- Small “phase tab” needed to clear field poly space inadvertently deleted during mask rule cleanup at PG.
- Result is scumming at litho, usually resulting in a poly short post etch (sometimes cleared by etch causing GEC).



Post-etch simulation predicts bridging, especially with misalignment



Small phase tab in the post-OPC output, inadvertently deleted at PG



Post PG output. Tab is missing and hammerhead will bridge to adjacent gate.

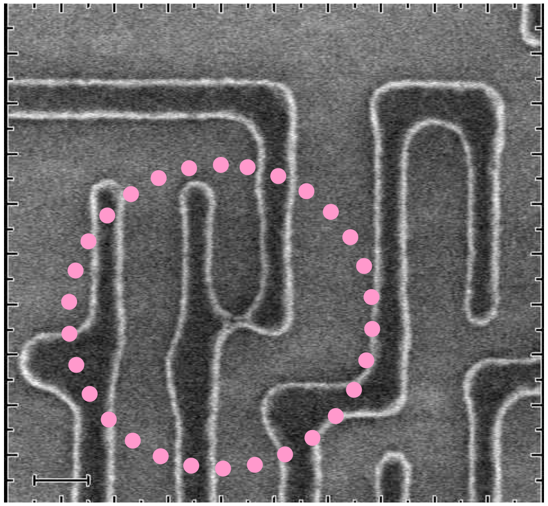
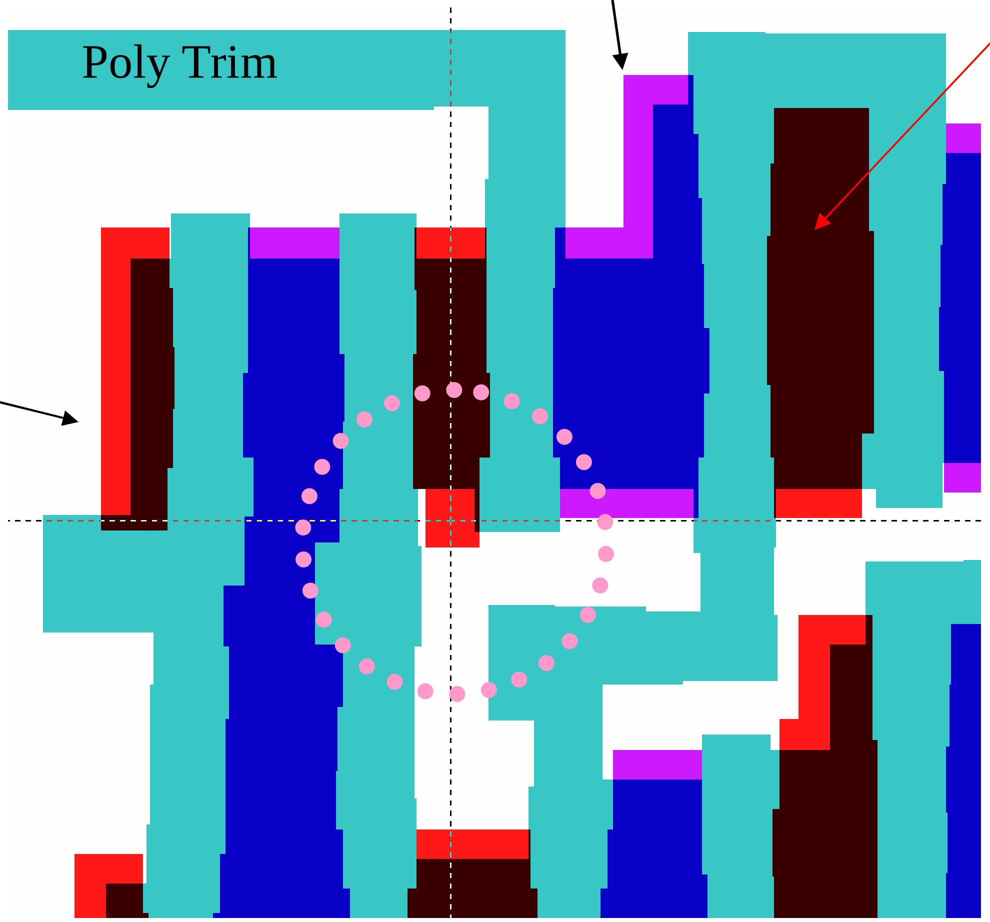


Photo data confirms bridging at same location, even at nominal conditions

Gate Short Root Cause for Bin 14 Failures

Design Database



Phase Zero

Phase PI
over Trim

Phase PI

Phase Zero
over Trim

Summary

- Rapid yield improvement can help with increased profits.
- Rapid yield improvement requires knowledge of testing, data mining, device physics, electrical fail site isolation and physical failure analysis.