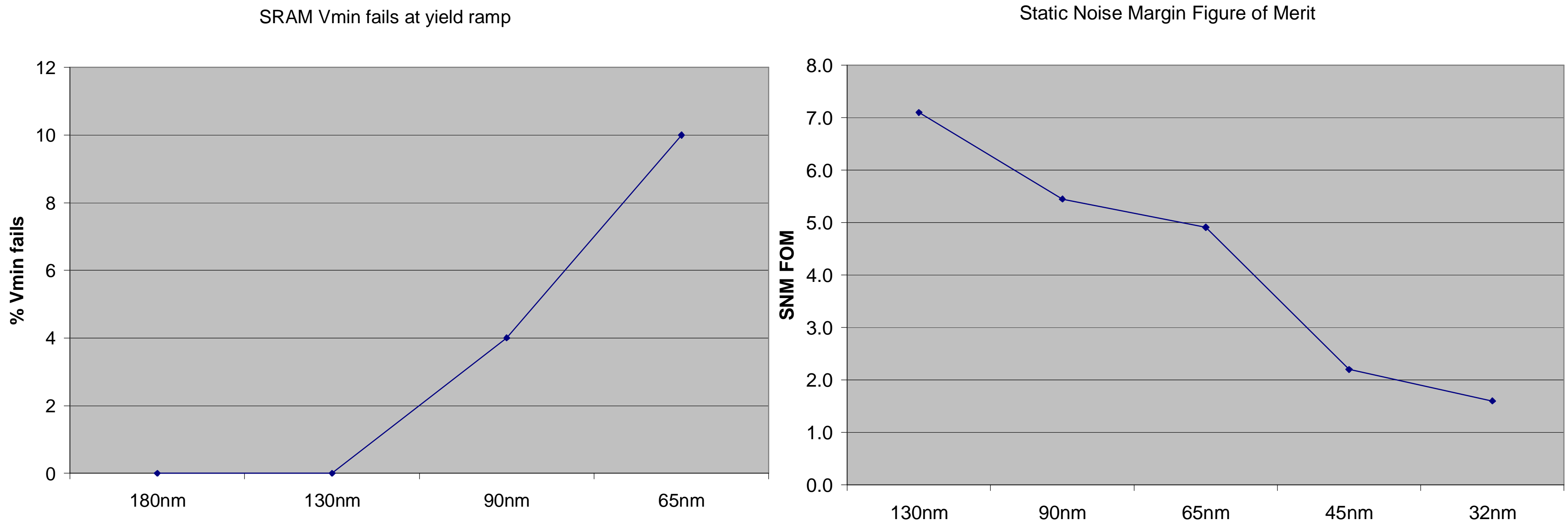
Presentation outline

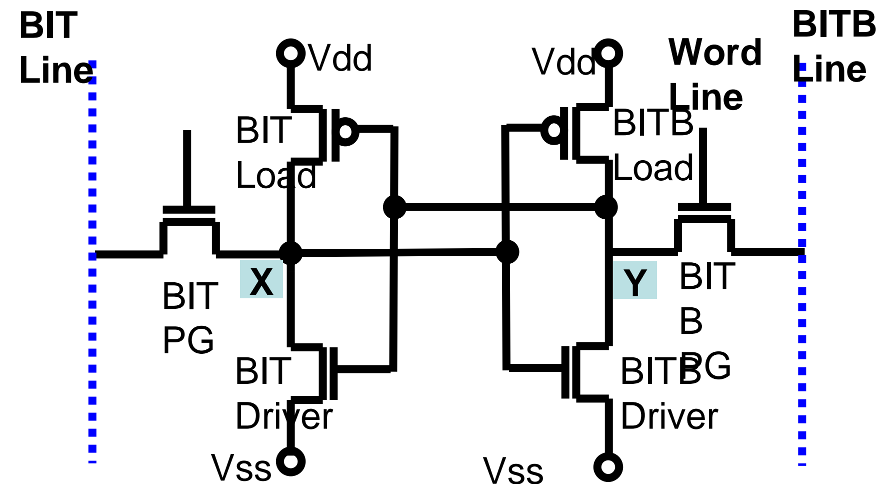
- Identification of hard and soft BIT failure modes in sub micron SRAM cells.
- Validation of design layout topology based on the SRAM BIT.

Problem statement



- As shrink occurs the SRAM Vmin fails increases and this trend is linked to a decrease in static noise margin (SNM).

SRAM design nomenclature



- When Bit line side of SRAM is zero, the cell is denoted to be at state zero.
- When Bit line side of SRAM is one, the cell is denoted to be at state one.

Test conditions

SRAM State	BIT Line Node X	BITB Line Node Y	Comment
Pass r0/w0/d0	0	1	Passes data 0 test
Pass r1/w1/d1	1	0	Passes data 1 test
Fails r0/w0/d0	1	0	Node X stuck at 1
Fails r1/w1/d1	0	1	Node Y stuck at 1

- To test whether the cell is at state 0 or 1 Integra Iflex was used with direct memory access capability.

Test Units

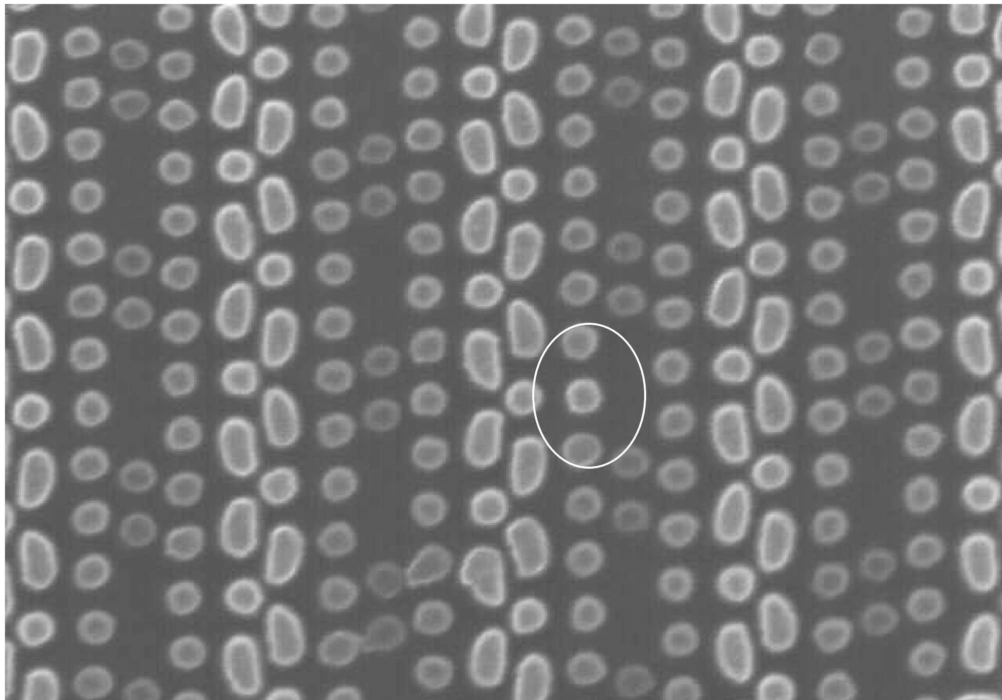
Case	**Fail mode**	**Data 0 or 1**
1	Fails R1/W1/D1 upto 0.91V	data 1
2	Fails R0/W0/D0 upto 0.91V	data 0
3	Fails across all voltages (R0/W0/D0)	data 0
4	Fails across all voltages (R1/W1/D1)	data 1
5	Fails Disturb 0 up to 1.2V	data 0
6	Fails disturb 1 up to 1.56V	data 1

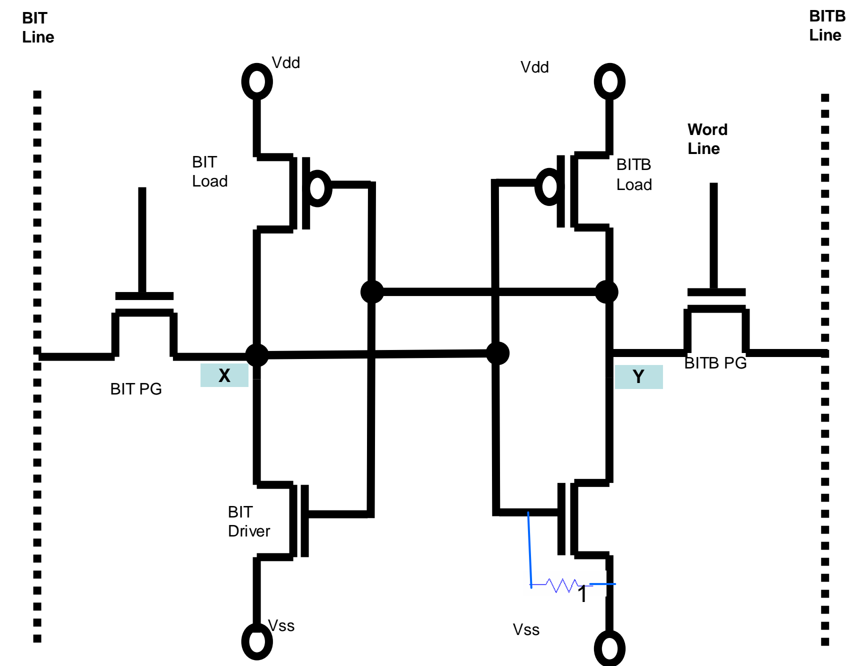
- 6 dies with 3 each of data 0 and data 1 fails.
- Voltage condition of the 6 fails also obtained.

Physical failure analysis

- PFA was performed on the 6 dies to see which node (X or Y) has flipped.

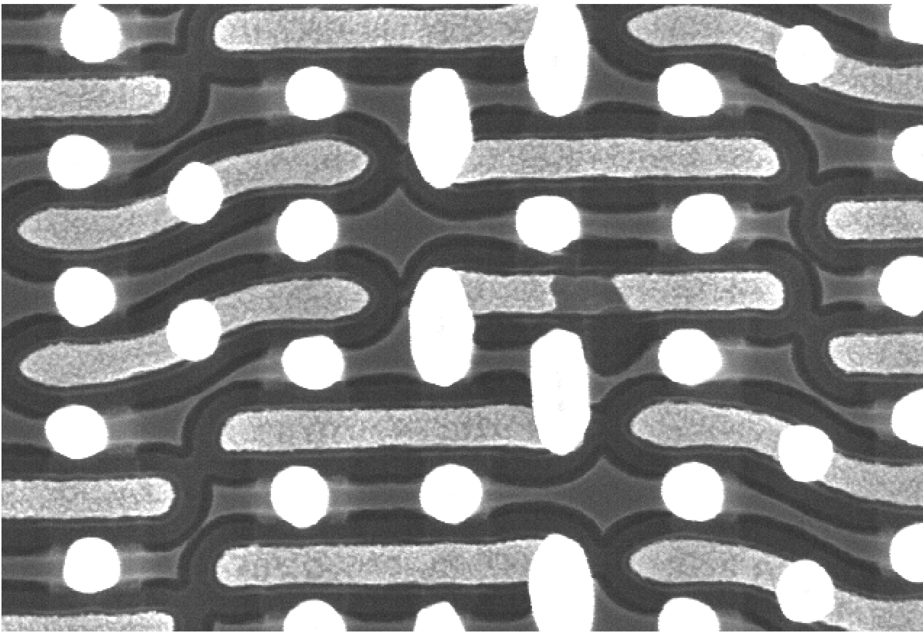
Case 1: Data 1 fail up to 0.91V

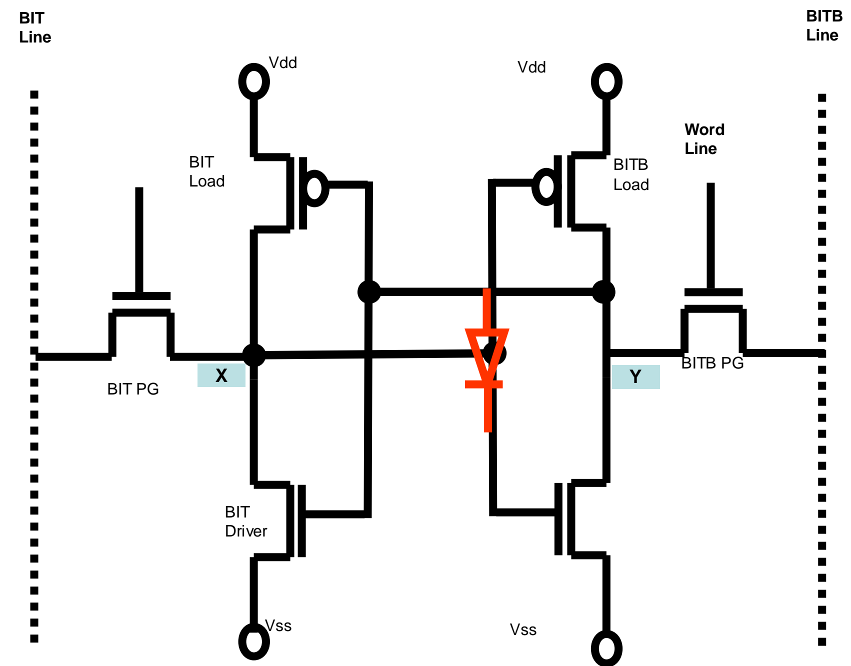




- The bitbar driver (pull down) transistor is never on. This makes node Y always 1 and node X always 0. Hence when one is written the BIT flips to zero (node x=0)
- Bright voltage contrast is due to a short between the gate and source in the bitbar side. This short makes the bitbar driver off making node Y high and node X low all the time. Hence when one is written, node X being low all the time, flips to zero – making a data 1 fail.

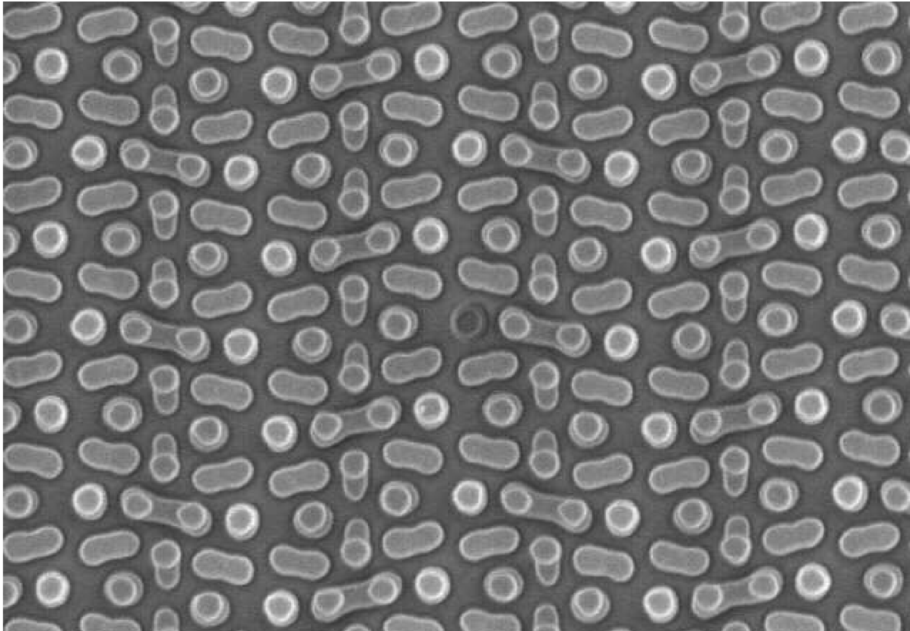
Case 2: Data 0 fail up to 0.91V

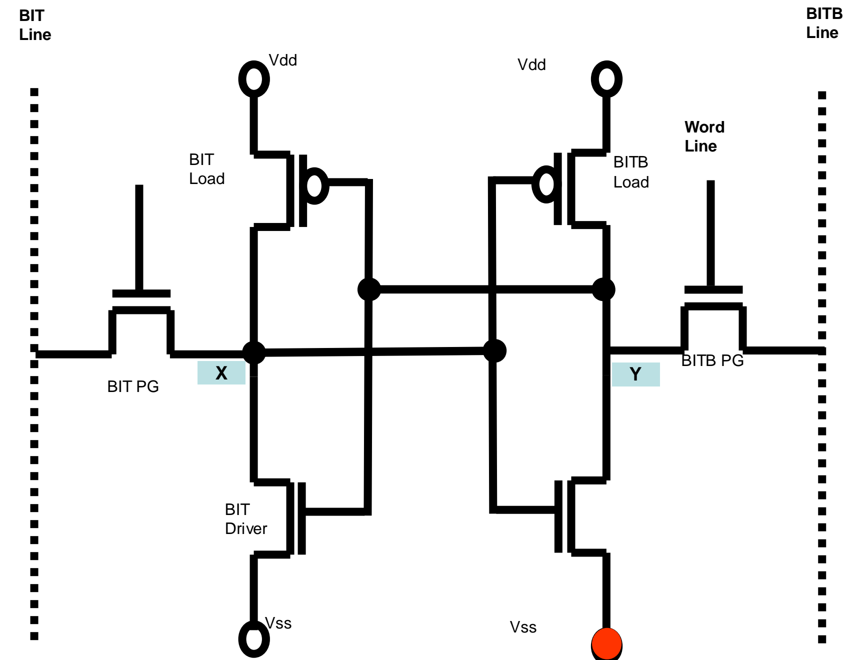




- With no ohmic resistance between the shared poly gates of load and driver; a diode is present, this makes the driver to be on all the time causing node Y to be 0. This causes node X to be 1 all the time. Hence when 0 is written the the BIT flips to 1.

Case 3: Data 0 fails all voltages



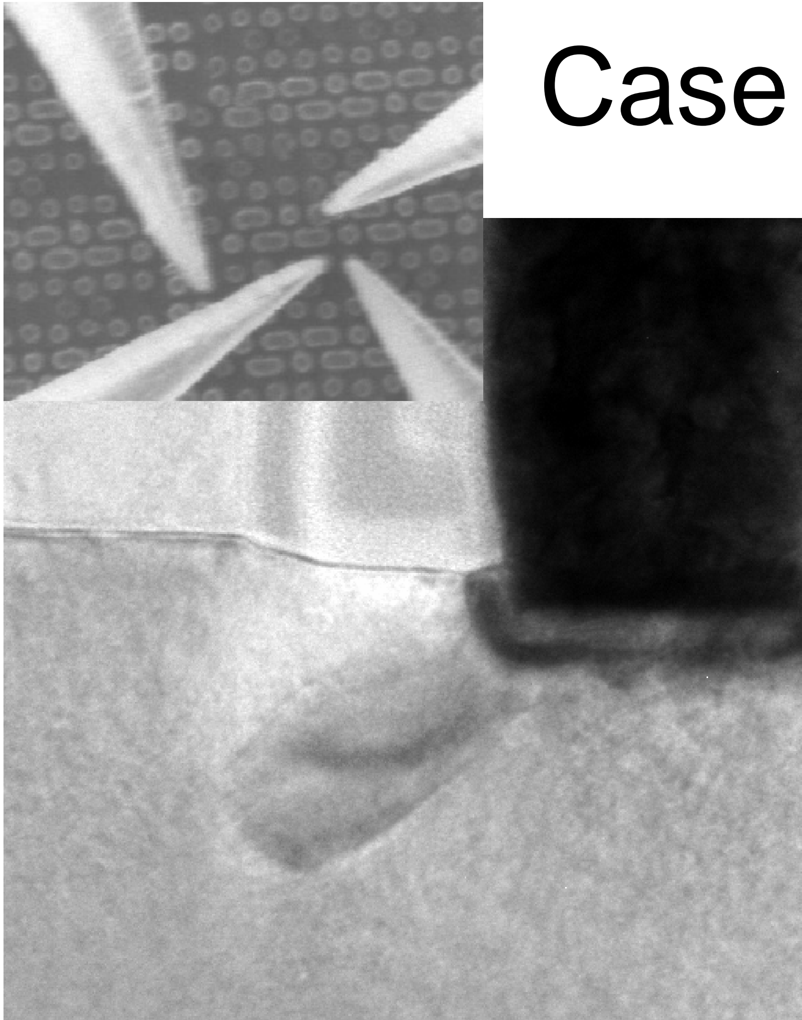


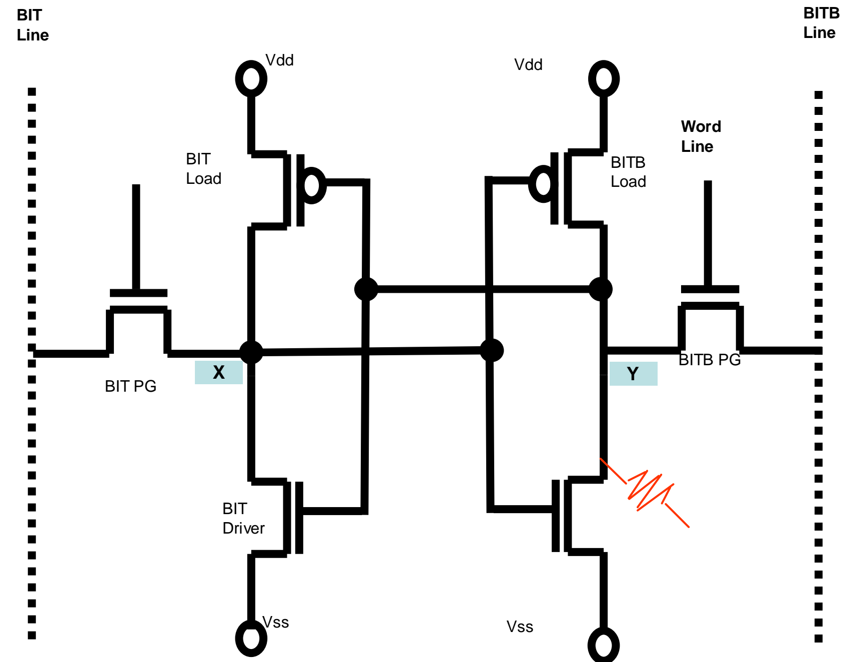
- This is a data 0 fail. A dark voltage contrast (open contact) is observed on the bitbar side. This is an open Vss contact on the bitbar side. This contact being open cause node Y to be low and node X to be high all the time. Hence when zero is written, the BIT flips to one.

Case 4: Data 1 fails all voltages

- This is a data 1 fail. Open contact due to residue underneath the contact observed. Node X is open making node X to be always zero thereby node Y to be one. Hence when one is attempted to be written, the BIT flips to zero.

Case 5: Disturb 0 up to 1.2V





- The fail is a data 0 fail. Pipe defect causing a short of the junction observed. The short is between drain and substrate (pipe defect) in the bitbar side. This causes node Y to be always low and node X to be always high. Hence when zero is written on the BIT, the node flips to high.

Case 6: Disturb 1 up to 1.56V

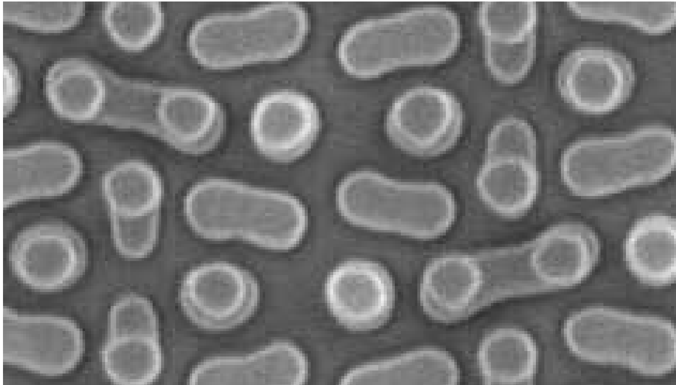
- The short is between the drain and substrate (pipe defect) in the bit side. This causes node X to be always low and node Y to be always high. Hence when one is written on the BIT, the node flips to low.

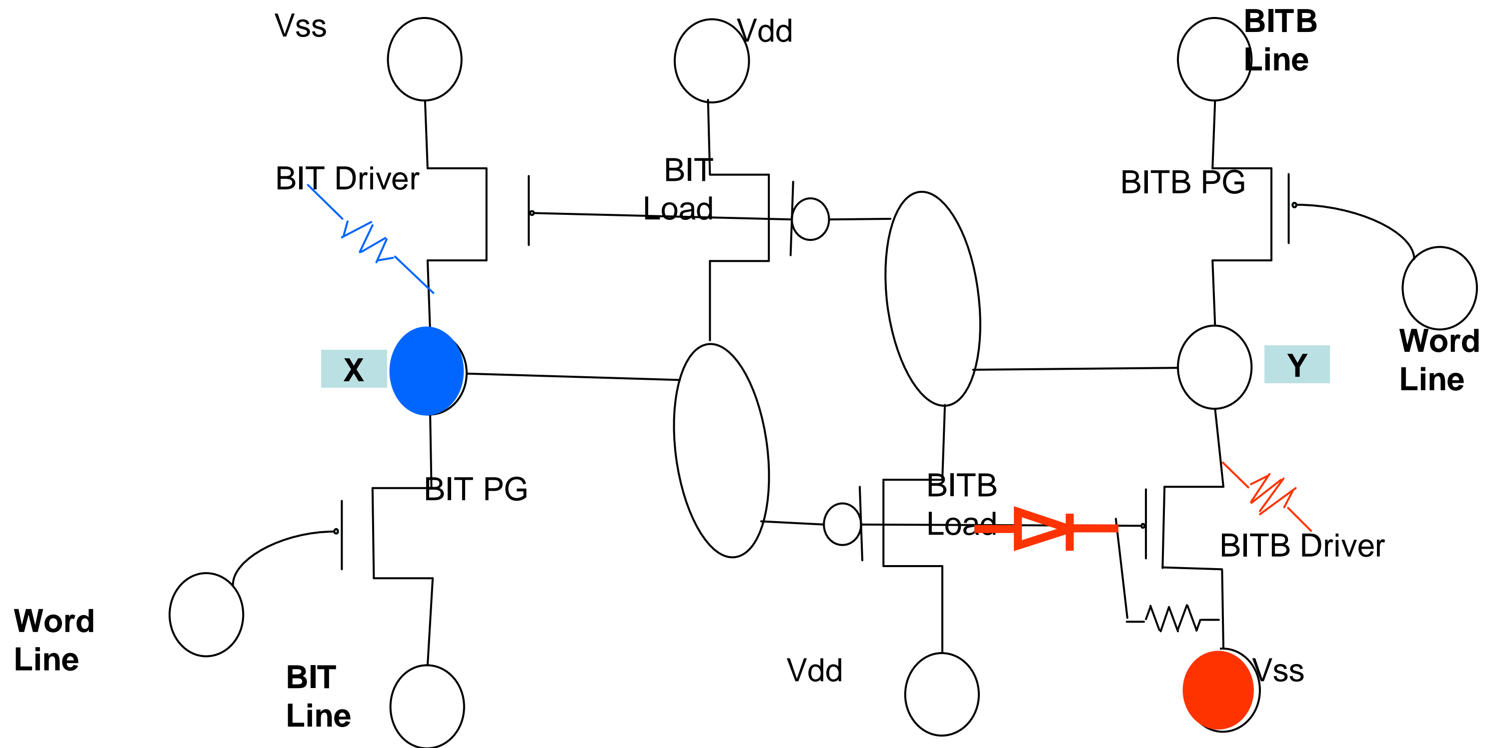
Summary

Data 1 fails in blue. Data 0 fails in red

- All 6 fails correlated to the Bit side state.

Using Cell orientation (physical)

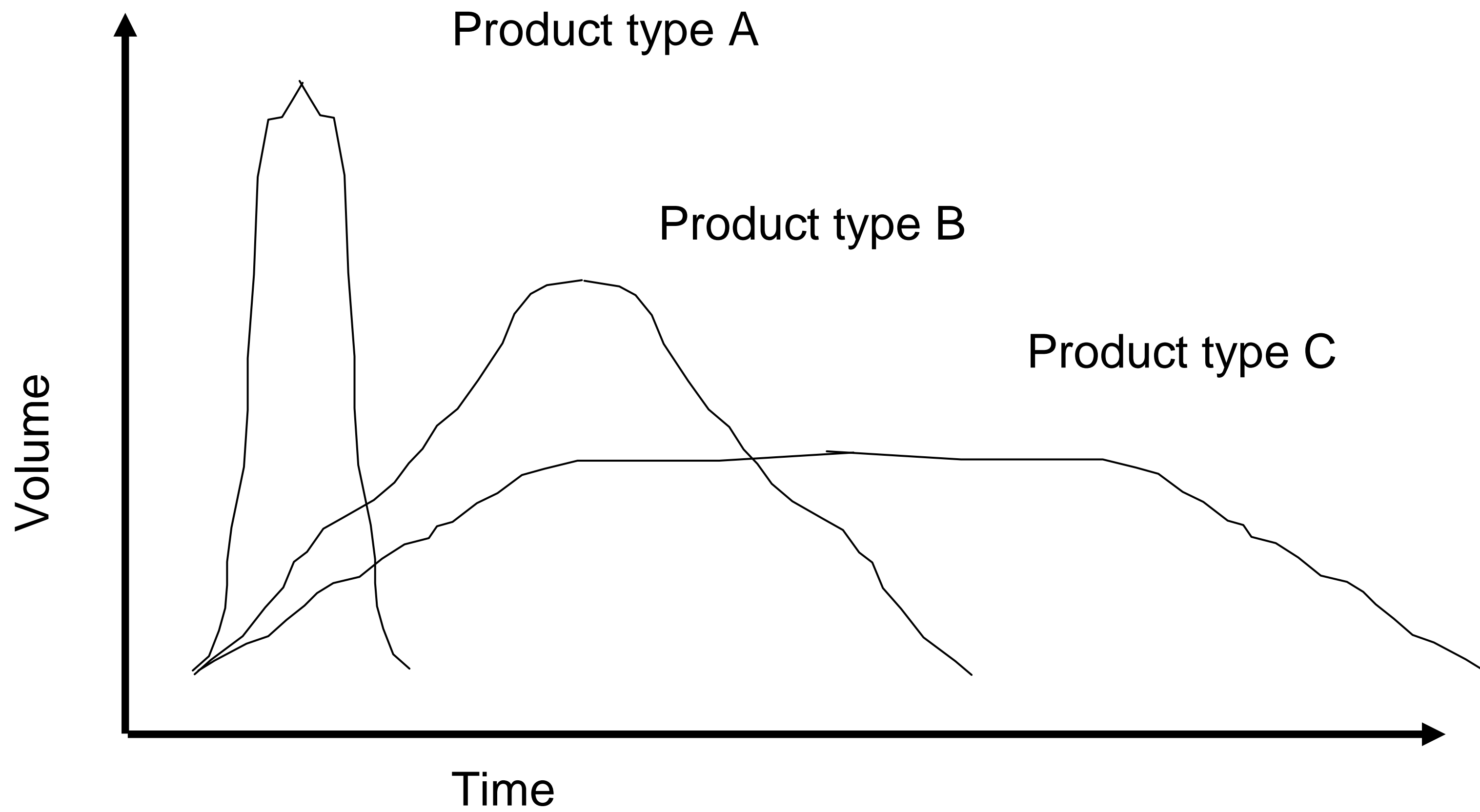




Conclusions

- Design methodology verified.
- Can use this for nano probing of transistors especially Vmin fails.
- Hard fails typically have a physical defect.

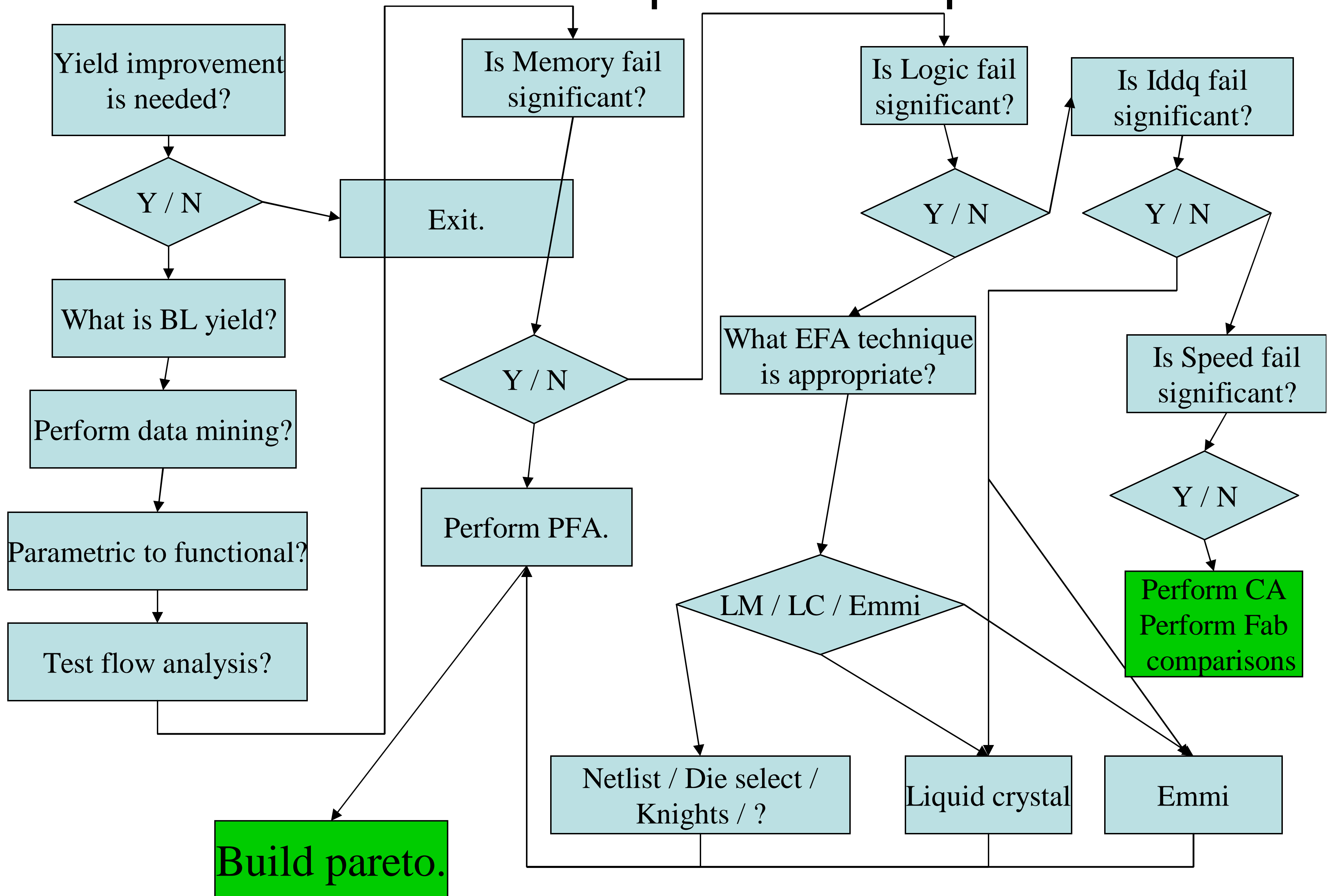
Product life cycle



Failure analysis Paradigm

- Design debug
  - FIB edits
  - Circuit analysis
- Yield improvement
- Reliability (qualification and life time predictions)
- Customer returns

Baseline Yield improvement process



Bipolar Differential Amplifier (Emitter Coupled Pair)

With resistive load.

Differential Input Voltage

$$v_{id} = v_{+} - v_{-}$$

Common Mode Input Voltage

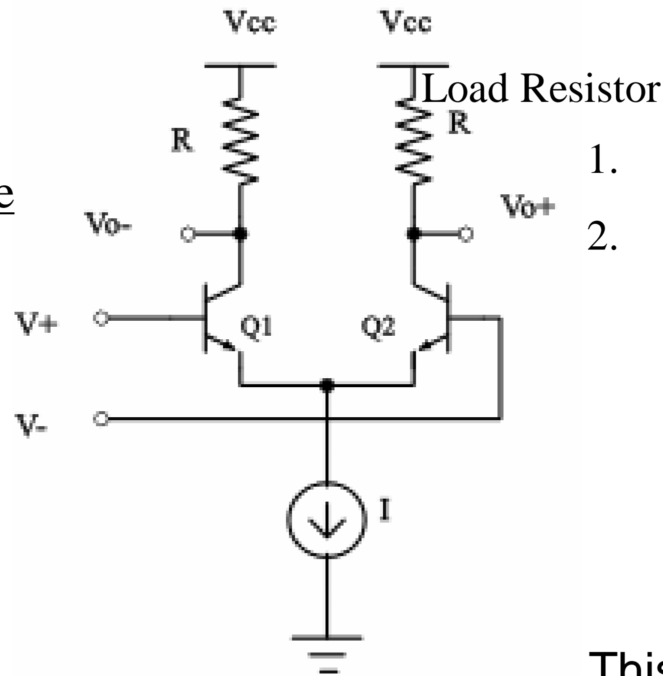
$$v_{ic} = \frac{v_{+} + v_{-}}{2}$$

Differential Output Voltage

$$v_{od} = v_{o+} - v_{o-}$$

Common Mode Output Voltage

$$v_{oc} = \frac{v_{o+} + v_{o-}}{2}$$



Load Resistor

Tail Current

Qualitative Operation.

1. Differential signals are amplified.
2. Common Mode signals are rejected.

This assumes Q1=Q2.
Layout and interdigitation can cause variation hence cause a shift in Vo+

Failure analysis requirements

- Knowledge of tools
  - microscopy, spectroscopy
  - Test tools – Teradyne, Keithley, bench
- Knowledge of statistics.
- Knowledge of process flows for the type of device or system (hardware / software).
- Knowledge of materials and its applications.